



**NMRA DCC Packet Encoder V2.0**

Copyright 2010 R D Godsey & Associates, Inc.

## NMRA DCC Packet Encoder

The encoder assembles, encodes and outputs NMRA S 9.1 DCC packets. The data encoded in the packets is supplied by another processor such as a PC or single board computer that forms the user interface and packet scheduler of an NMRA Command Station.

Only the data length and data itself are written to the encoder. The external process needs to monitor the encoder 'busy' signal by polling or preferably by interrupt. When the encoder buffers are empty (not busy), data can be loaded by parallel or serial interface. If no data is in the encoder buffers, it outputs DCC encoded '1's.

The general DCC packet format consists of a frequency encoded serial stream:

preamble, <data>, crc

Digital 1s are represented by 1 cycle at 116 microseconds and 0s by 1 cycle less than or equal to 232 microseconds. Each cycle consists of equal time half cycles. The DCC packet consists of a preamble of at least 10 encoded 1s, 2 to 4 data bytes and an error check byte all separated by an encoded 0. Packet transmission time varies from a minimum of a little more than 5.5 milliseconds to over 10. New data must be written to the encoder at a minimum of 3 bytes (count and 2 data bytes) every 5 milliseconds.

Data can be written to the packet encoder by parallel or serial interface. Options are selected at reset by the state of the configuration pins.

### Encoder Configuration:

The parallel Interface is enabled if pin 3 (TxD) is at 0 volts. If pin 3 is left open, the serial interface is enabled. In the serial mode, pin 12 selects a BAUD rate of 19.2K if left open or 9.6K if at 0 volts. Pin 13 selects 8 bit frame if left open or 9 bit 8051 'ID' frame if at 0 volts.

## Timing Diagrams

Signal direction is from the encoder's perspective.

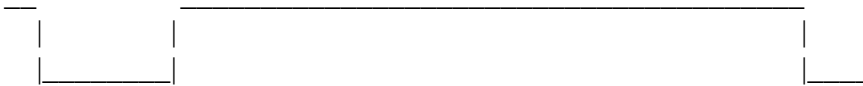
Parallel Data Interface:

Pin 3 is grounded enabling the parallel data transfer mode.  
Signals and timing are shown sending an 'IDLE' command:

Length: 002H  
Data 1: 0FFH,  
Data 2: 000H

Timing for Parallel interface:

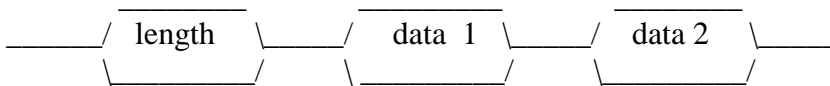
Write - output pin 6 (INT0)



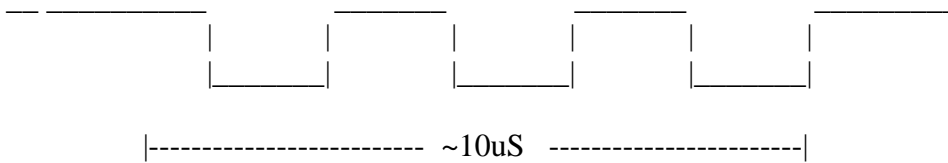
Busy/Ready - input pin 11 (P3.7)



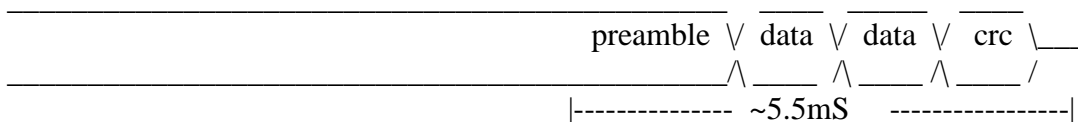
Data - input (D0-D7 on pins 12 through 19 respectively (P1[0..7])



Transfer Acknowledge - output pin 7 (INT1)



DCC Output - output pin 8 (T0)

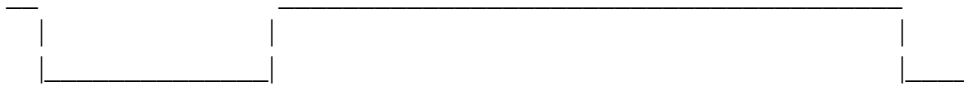


## Serial Data Interface

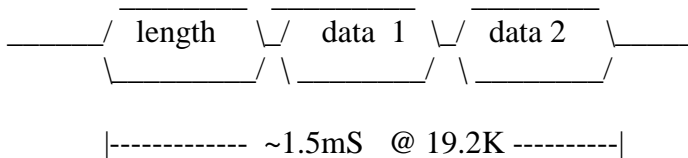
Pin 3 is left open enabling the serial data mode. Pin 12 and 13 are open setting 19.2K and 8 bit frame.

Timing for Serial interface:

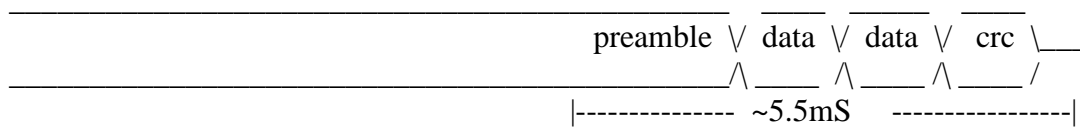
Busy/Ready - output pin 6 (INT0)



Serial Data - input pin 2 (RxD)



DCC Output – output pin 8 (T0)



The DCC output is connected to most available DCC Power Stations through appropriate drivers. See NMRA RP 9.12 for standard power station interface specification.

In RDG&A command station designs, 'Ready' is connected to an interrupt on the station processor. The interrupt service routine outputs active DCC data from a string of receiver descriptors maintained by the user interface software.